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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,131	02/02/2004	Suresh Balasubramanian	TI-36687	5630

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EXAMINER	
WENDLER, ERIC J	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/768,131	BALASUBRAMANIAN ET AL.	
	Examiner	Art Unit	
	Eric Wendler	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: word line 122-1, as mentioned on page 9, line 5; bit line 113-M, as mentioned on page 9, line 9; column 113-4, as mentioned on page 10, line 2; clock generator 320, as mentioned on page 20, line 16. They also include the following reference character(s) not mentioned in the description: Figure 1A, 175; Figure 4, 411. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: the disclosure is in compliance with (b) as mentioned below, but there is no serial number included because it was unassigned at the time of the application. The co-pending application number is 10/768098. Please correct to include this number. Also, as

mentioned below in (g), a brief summary of the invention is required in the specification. This section is missing in the current specification.

Appropriate correction is required.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(g) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

Claim Objections

3. Claims 1-21 are objected to because of the following informalities:

Claim 1, line 4: lacks antecedent for "said actual memory," as the antecedent as stated in line 2 is "actual memory array". Examiner suggests changing "said actual memory" to -- said actual memory array --.

Claim 1, line 9: Delete the word "an" before "another".

Claim 3, line 1: lacks antecedent for "said dummy memory," as the antecedent as stated in claim 1 is "dummy memory array." Examiner suggests changing "said dummy memory" to -- said dummy memory array --.

Claim 4, line 1: refers to "said array." However, there are two possible antecedents for this phrase: "dummy memory array" and "actual memory array." This language is

ambiguous and indefinite; the applicant must clearly indicate which array is being referenced.

Claim 7, line 1: the word "transistor" should be plural in line 1. Examiner suggests changing "transistor" to -- transistors --.

Claim 7, line 1: refers to "said transistors." However, there are two possible antecedents for this phrase: "array of transistors" and "column of transistors." This language is ambiguous and indefinite; the applicant must clearly indicate which array is being referenced.

Claim 10, line 2: lacks antecedent for "said actual memory," as the antecedent as stated in claim 1 is "actual memory array". Examiner suggests changing "said actual memory" to -- said actual memory array --.

Claim 15, line 1: lacks antecedent for "said dummy memory," as the antecedent as stated in claim 1 is "dummy memory array." Examiner suggests changing "said dummy memory" to -- said dummy memory array --.

Claim 16, line 1: refers to "said array." However, there are two possible antecedents for this phrase: "dummy memory array" and "actual memory array." This language is ambiguous and indefinite; the applicant must correct to clearly indicate which array is being referenced.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 5, 14, and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 5, 14, and 17, the phrase "similar to" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3-5, 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by the US Patent to Yokozeki (6,741,505).

In terms of claims 1 and 14, Yokozeki shows, in Figure 11, an actual memory cell array (100), a decoder circuit (120) to retrieve a signal from the actual memory array, an actual sense amplifier (106) to sense the signal as a bit, a latch (107) latching said bit at a time point specified by a latch enable signal, a dummy memory array (211, 212, 213) offering a load when accessed, and a dummy sense amplifier (206) sensing a signal received when the dummy memory array is accessed. Yokozeki also refers to these components in column 4, lines 20-24; column 4, lines 24-28; column 4, lines 45-49; column 4, lines 49-53; and column 7, lines 44-45, respectively. A positive

correlation between the load of the dummy memory array and a delay in the generation of another signal is taught in column 9, lines 39-52.

As for claims 3 and 15, Yokozeki shows, in Figures 10A-10B and column 12, lines 58-60, a dummy memory array comprised of transistors.

As for claims 4 and 16, Yokozeki shows, in Figure 14 and column 14, lines 65-67, and column 15, lines 1-13, a dummy memory array comprised of a column of transistors.

As for claims 5 and 17, Yokozeki describes the actual memory array in column 2, lines 11-13. Yokozeki goes on to describe the dummy memory array in column 2, lines 25-29. The actual memory array and the dummy memory array are described as being comprised of cells at the intersections of equal numbers of bit lines and word lines. Since it is well known in the art that memory arrays are comprised of columns of transistors, Yokozeki describes a dummy memory array containing less than or equal to a number of transistors as a number of rows in the actual memory array.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokozeki in view of the US Patent to Murakami (6,912,101).

Yokozeki teaches all of the claimed elements, as disclosed above, except for the memory system being implemented in a same die. Murakami teaches in Column 1, lines 28-44, that many advantages arise from implementing a memory system in a single die. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use the single die of Murakami to implement the memory system of Yokozeki in order to enjoy the convenience of the advantages taught by Murakami. Murakami teaches other things that are common to the field of endeavor, including references to DRAMs, MPUs, and serial ROMs.

10. Claims 6 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokozeki in view of the US Patent to Keeth (6,243,311).

Yokozeki teaches all of the claimed elements, as disclosed above, except each of the columns of transistors in the dummy memory array is of higher drive strength than the drive strength of the transistors in the actual memory array. Keeth teaches, in Column 9, lines 52-56, the use of transistors of higher drive strength in order to achieve a faster equilibrium between digit lines. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use the high drive strength transistors of Keeth to implement the memory system of Yokozeki in order to enjoy the advantage taught by Keeth. Keeth teaches other things that are common to the field of endeavor, including references to memory arrays that are comprised of arrays of transistors.

Claims 7 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokozeki in view of the US Patent to Keeth (6,243,311).

Yokozeki teaches all of the claimed elements, as disclosed above, except that each of the transistors is a NMOS transistor. Keeth teaches, in Column 9, lines 52-56, the use of NMOS transistors because the higher drive strength will allow one to achieve a faster equilibrium between digit lines. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use the NMOS transistors of Keeth to implement the memory system of Yokozeki in order to enjoy the advantage taught by Keeth. Keeth teaches other things that are common to the field of endeavor, including references to memories comprised of arrays of digit lines, and efforts to reduce die size.

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokozeki in view of the US Patent Application Publication to Sheffield (2004/0064661).

Yokozeki teaches all of the claimed elements, as disclosed above, except that the actual memory array comprises a compiler memory. Sheffield teaches, in paragraph 0014, page 2 of the specification, that different compiler memories can be accommodated in the same manner as the said actual memory array. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use the compiler memories of Sheffield to implement the memory system of Yokozeki, in order to allow the memory system to be compatible with variable sizes of arrays. Sheffield teaches other things that are common to the field of endeavor, including a memory system comprised of a memory array, row and column decoders, and a tracking circuit.

12. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yokozeki in view of the US Patent to Shirley (5,657,277), and further in view of the US Patent to Perrott (6,856,206).

Yokozeki teaches all of the claimed elements, as disclosed above, except that the dummy memory array and dummy sense amplifier are contained in a tracking circuit, and that the tracking circuit is implemented without reference signals. Shirley teaches, in Column 4, lines 47-59, a tracking circuit that contains a dummy memory array and dummy sense amplifier. Perrott teaches, in Column 1, lines 54-59, that it would be desirable to have a system that can acquire a clock signal without having to use a reference signal. It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use the tracking circuit of Shirley and the system without reference signals of Perrott to implement the memory system of Yokozeki, in order to allow for a memory system that achieves high access rates and is less complex and costly. Both Shirley and Perrott teach other things that are common to the field of endeavor. Shirley teaches that the tracking circuit is used to monitor word line voltages in a DRAM. Perrott teaches the use of a system that includes a sense amplifier that amplifies signals.

Allowable Subject Matter

13. Claims 8-11 and 20-21 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

With respect to claims 8 and 20, while the use of a current mirror in tracking circuits and memory systems is well known in the art, the prior art of record does not show the limitation of the detailed structure of the dummy and actual sense amplifiers, as stated in claims 8 and 20, comprising a first transistor having a drain terminal connected to a supply voltage and a gate terminal connected to a sense enable signal; a drain terminal of both of said second transistor and said third transistor being connected to a source terminal of said first transistor; a resistive load connected to a source terminal of said third transistor at a second node; an inverter having an input path connected to said second node; and a fourth transistor having a drain terminal connected to said first node and a gate terminal connected to said sense enable signal.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Chang (6,285,604), Tani et al (6,459,640), Tsuchiya et al (4,783,764), and Ong et al (5,465,232). All these references disclose memory systems similar to that of claim 1.

15. When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating the appropriate paragraphs.

16. A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 8 AM - 4:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached at (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJW
8/9/05

8/12/05

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